A Comparative Study of Conventional Solder Bump and Copper Pillar Bump in Flip Chip Technology using Computational Fluid Dynamics

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Abstract. Flip chip technology is one of the common electronic packaging techniques used in the electronic industry. Before, the solder bump flip-chip bonding is used to provide the electrical connections and mechanical supports to the assembly. However, due to the fast-paced nature of technology, electronic packaging technique has become more challenging and complicated. The demand for smaller chip and interconnection joints causes the bottleneck of the conventional flip-chip technology. In order to fulfill the rising demand from the emerging market, a copper (Cu) pillar bump with a solder cap is proposed to replace the conventional solder bump. Due to the electrical and mechanical properties of Cu, it can improve the electrical performance of interconnection joint and provide mechanical support to the package. In this paper, ANSYS Fluent is used to develop the models of the conventional solder bump and Cu pillar bump. The thermal behaviour of interconnection joint during solder reflowing process is simulated. The simulation results indicate that the heat transfer of Cu pillar bumps in the reflow oven is better than conventional solder bumps.

INTRODUCTION

The electronics industry consists of telecommunications, networking, electronic components, industrial electronics and consumer electronics. Within the consumer electronics market, the market segmentation is divided into five segments including televisions, radios and multimedia, peripheral devices, drones, smartphones and computers. The high demand of electronics industry has driven up the demand for the semiconductors industry due to the function of semiconductors which act as an essential part of electronic devices.

In the semiconductors industry, one of the commonly used semiconductor packaging techniques is the flip chip technology. The flip chip technology is described as a chip is attached to the substrate or other chip by various interconnect materials and techniques (Lau, 2016). Because of the rapid miniaturization in semiconductor packaging, small-sized solder joints are preferrable and the bump size shrinks to form fine pitch below 100μm. The conventional flip chip technology has reached its limitation and the copper (Cu) pillar technology has been used suggested to replace the conventional flip chip technology due to its superior electrical and thermal properties (Henderson, 2012).

The comparison between the conventional solder bump and the copper pillar technology in the flip chip technology will be discussed throughout this paper.

Flip Chip Technology

In the early 1960s, the flip chip technology was introduced by IBM for their solid logic technology, which later became the logical foundation of the IBM System/360 computer line, and it is widely applied in the electronic packaging industry due to its advantages (Lau, 2016; Tsai et al., 2017). Figure 1(a) shows the schematic diagram of a flip chip bonding assembly, a chip is attached to the metal pad of substrate or another chip by facing down towards the metal pad.

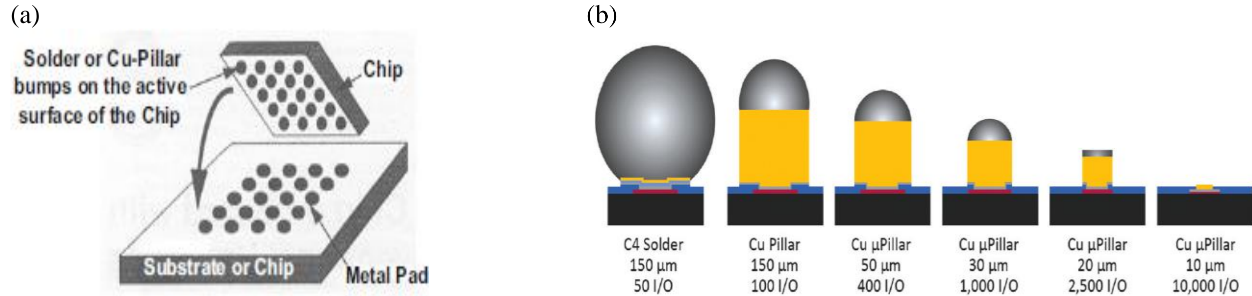


Figure 1: (a) Schematic Diagram of Flip Chip Assembly (Lau, 2018), (b) Flip Chip Interconnect Bumping from C4 Solder to Direct Cu (Gregorich & Gu, 2019)

Based on Tsai et al. (2017), the chip interconnection bumps technology can be characterized into three generations as shown in Figure 1(b). The first generation, the controller collapse chip connection (C4) bumps utilized high-lead solder bump with a bump pitch over 130µm. Second generation which is named as micro bump or chip connection (C2) bumps, is currently applied in the packaging industry and have a bump pitch ranging from 40 to 130µm. The third generation which is known as three-dimensional integrated circuit (3DIC) assembly has a bump pitch which has been reduced to be smaller than 30µm.

The flip chip technology offers a number of advantages, including the higher Input/Output (I/O) count, shorter connections, mechanical support and thermal dissipation. The flip chip bonding can have I/O all over the chips; thus, the interconnection is formed between I/O of device chip and I/O of substrate with the aid of soldering. Based on the Table 1 which shows the comparison between C4 bumps and C2 bumps, the thermal conductivity and electrical resistivity of copper pillar bump are more superior than those of solder (Lau, 2016; Lau, 2018). The copper pillar bumps able to offer a good thermal and electrical performances when compared to solder bumps.

Table 1: Comparison Between C4 Bumps and C2 Bumps (Lau, 2018)

Structure	Major Material	Thermal Conductivity (W/m K)	Electrical Resistivity (µΩm)	Pad Pitch	Self-Alignment
C4 Bump	Solder	55-60	0.12-0.14	Large	Large
C2 Bump	Copper	400	0.0172	Small	Small

However, the solder volume of cap in the copper pillar bump is much smaller (Long et al., 2020). The surface tension of solder cap may not enough to perform the self-alignment of the copper pillar bump with solder tip, resulting in the reliability problem of connection joints (Lau, 2016).

Reflow Soldering Process

Surface Mount Technology (SMT) processes begin with the solder paste printing process, then followed by the component mounting process. The solder paste is dissipated on a substrate using a stencil and the electrical

components are placed on the substrate. The assembly is then sent to a reflow oven to undergo the reflow soldering process (Rusdi et al., 2018; Asghar et al., 2020). In the oven, the assembly is travelled into different heating zones, namely preheating, soaking, reflow and cooling stages.

Based on Briggs and Lasky (2012), the reflow soldering region begins after 180s into the heating period, and the reflow soldering process will last for approximately 40s to 80s. Najib et. al (2015) claimed that the reflow time range is between 160s to 220s. Srivalli et al. (2015) set the reflow oven according to the valid temperature zones as shown in Figure 2(b), where the reflow time range is between 220s to 280s. Also, Tao et al. (2017) stated that the temperature profile of the SMT Scope is a standard lead-free temperature profile for SAC305, it is estimated that the reflow stage occurs between the time 125 to 185s. Long et. al (2020) simulated the temperature profile of the Cu pillar bump and showed that the time range for reflow soldering process is 250s to 300s.

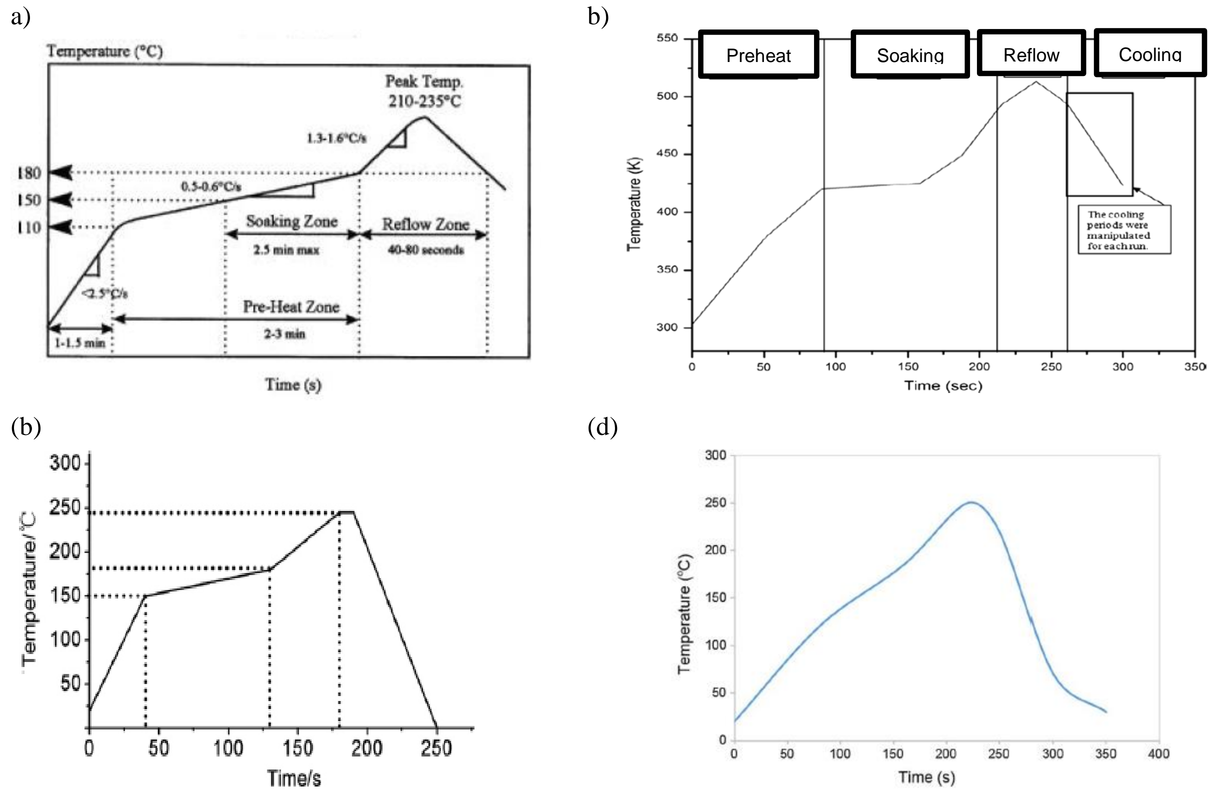


Figure 2: Temperature Profile of The Reflow Process: (a) Briggs & Lasky (2012), (b) Srivalli et al. (2015), (c) Tao et al. (2017), (d) Long et al. (2020)

There are numerous numerical approaches that can be used to simulate the reflow soldering process, including Finite Element Method (FEM) and Finite Volume Method (FVM). Through FVM, Najib et al. (2015) demonstrated the air circulation mechanism during the reflow soldering process of solder bump. Thermal behaviour study of solder joint has been conducted by Srivalli et al. (2015) using FVM and Esfandyari et al. (2017) using FEM. Besides, Deng et al. (2016) used FEM to develop the temperature distribution of sistem-in-package (SiP) assembly to design a thermal profile with minimal gradient. Tang et al. (2018) simulated the temperature zones in the reflow oven and it was found that the temperature distribution was uneven after various temperature zones. For Cu pillar bump, most of the analysis has been done using FEM. Stress simulation was conducted and stress distribution of the Cu pillar bump was predicted to investigate the crack formation (Chen et al,2014; Che et al, 2015; Ma et al, 2016; Long et al, 2020; Sun et al, 2020)

The numerical simulation is important as it is a cost-effective and time-saving tool that helps to improve the reflow process. From the findings from different researchers, it is clear that the majorities of the studies which are done on Cu pillar bump are FEM and limited to stress analysis. Thus, in this paper, both the solder bump and Cu pillar bump are compared, and their temperature profiles during reflow soldering are simulated using ANSYS Fluent.

METHODOLOGY

The purpose of introducing the numerical approaches in the SMT field is to save cost and time from experimental work. The numerical approaches such as FEM and FVM can be used to simulate the reflow soldering process and solve the real-world problems in the electronic industry. The simulation model can be used to predict the temperature distribution for the soldering material together with the chip and substrate, as well as predict the interconnection joint condition.

The methodology developed in this study is used for predicting the temperature distribution in an oven, and the simulation process is shown in Figure 3. The basic idea is to set up a new method to analyse the difference between the interconnection using conventional solder joints and Cu pillar bumps inside the oven using ANSYS Fluent, which is a FVM-based software (Abdul Aziz, et al 2013, 2014, 2015). Figure 4 illustrates the schematic diagrams of the model, consisting of an oven, a ball grid array (BGA) chip, a substrate, heater tubes and solder joints or copper pillar bumps. Two models are developed based on the currently known requirements shown in Table 2.

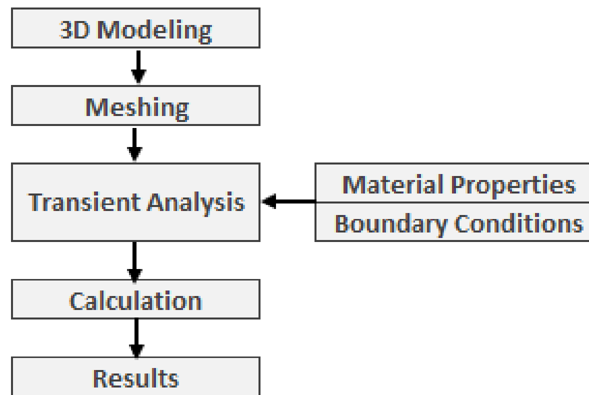


Figure 3: Simulation Process Flow

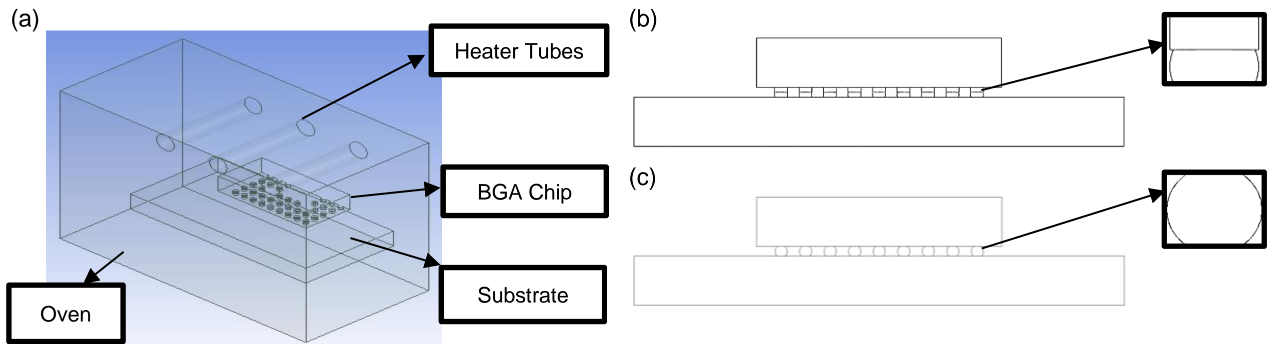


Figure 4: Schematic Diagrams of Model: (a) Isometric View of Model, (b) Simplified Copper Pillar Bump with Solder Cap Model, (c) Simplified Solder Bump Model

Table 2: Dimension of Models

Material	Dimension (mm)
BGA Chip	5 x 5 x 1
Copper Pillar with Solder Cap	Height: 0.1
	Diameter: 0.25
SAC305 Solder	Height: 0.1
	Diameter: 0.25
Substrate (Copper Pad)	10 x 10 x 1
Oven	16 x 16 x 8.1

After building the 3D model, the model is sliced into half and the sectional plane is set as symmetry plane. The meshing is done using Ansys Fluent Meshing as shown in Figure 5, local sizing is applied on Cu pillar, solder cap, BGA chip and substrate. Next, surface mesh and volume mesh are applied on the whole structure. By referring to the mesh metrics as shown in Table 3, the generated meshes are checked and the mesh qualities are reported in Table 4. It is important to generate a mesh with good quality, a good mesh increases the accuracy of the simulation result.

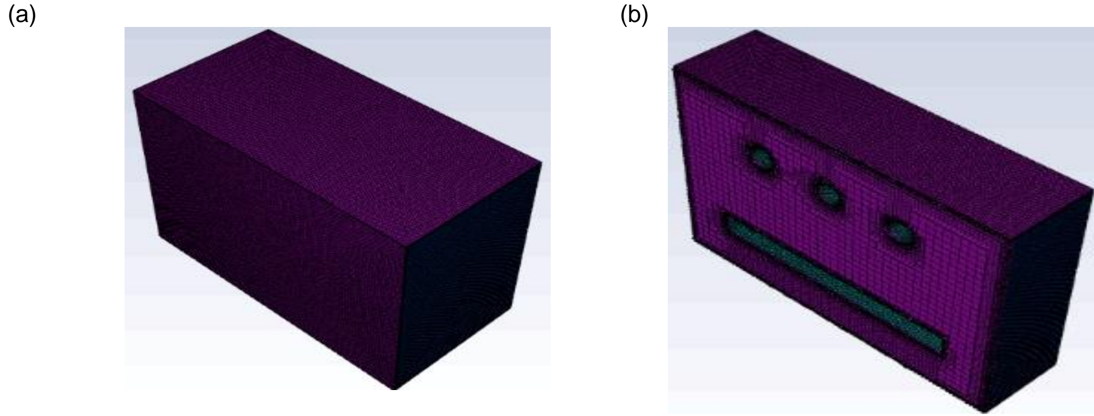


Figure 5: Model Meshing (a) Overall Structure, (b) Sliced Structure

Table 3: Mesh Metrics (Sherrard, 2020)

	Skewness Mesh Metrics	Orthogonal Quality Mesh Metrics
Excellent	0 – 0.25	0.95 – 1.00
Very Good	0.25 – 0.50	0.70 – 0.95
Good	0.50 – 0.80	0.20 – 0.69
Acceptable	0.80 – 0.94	0.15 – 0.20
Bad	0.95 – 0.97	0.001 – 0.14
Unacceptable	0.98 – 1.00	0 – 0.001

Table 4: Mesh Check and Mesh Quality

	Conventional Solder Bump	Cu Pillar Bump with Solder Cap
Number of Nodes	2198667	4453970
Number of Cells	708065	1479570
Maximum-Skewness	0.77810365 (Good)	0.7988395 (Good)
Minimum Orthogonal Quality	2.21896e-01 (Good)	3.00520e-01 (Good)

Then, transient analysis is conducted by setting up the material properties of oven and electrical components as shown in Table 5, as well as the boundary conditions. The air velocity in the inlet is set as 1m/s and the pressure at the outlet is 101,325 Pa. The heater tubes in the oven are set as discrete ordinations (DO) radiation model and user-defined function (UDF) is created for the reflow soldering process. The UDF is interpreted in Ansys Fluent software and it changes according to different durations at the reflow soldering stage. A simulation for the time period from t = 0 to t = 300s is run, the number of the time step is set as 300 and the time step size is set as 1 before running the simulation.

Table 5: Mechanical Properties

Material	Density (kg/m^3)	Thermal Conductivity (W/mK)	Specific Heat Capacity (J/kg)
BT Substrate	1700	0.2	920
SAC305 Solder	7380	58	366
Copper	8978	3876	381
Aluminium	2719	202.4	871

RESULTS & DISCUSSION

Temperature Distribution

In the process, the heat is transferred to the substrate with BGA assembly from a heated wall. In the heat transfer, the interconnection joints like solder joint or copper pillar bump with solder cap slowly absorb the heat from the substrate and start to melt according to the thermal profile setting (Srivalli et al., 2015). The amounts of heat distributed throughout the interconnection joints at different durations of the reflow stage are obtained from the numerical simulation. Figures 6 and 7 show the temperature distribution contour comparison of conventional solder bump and copper pillar bump with solder cap at different durations of the reflow soldering process.

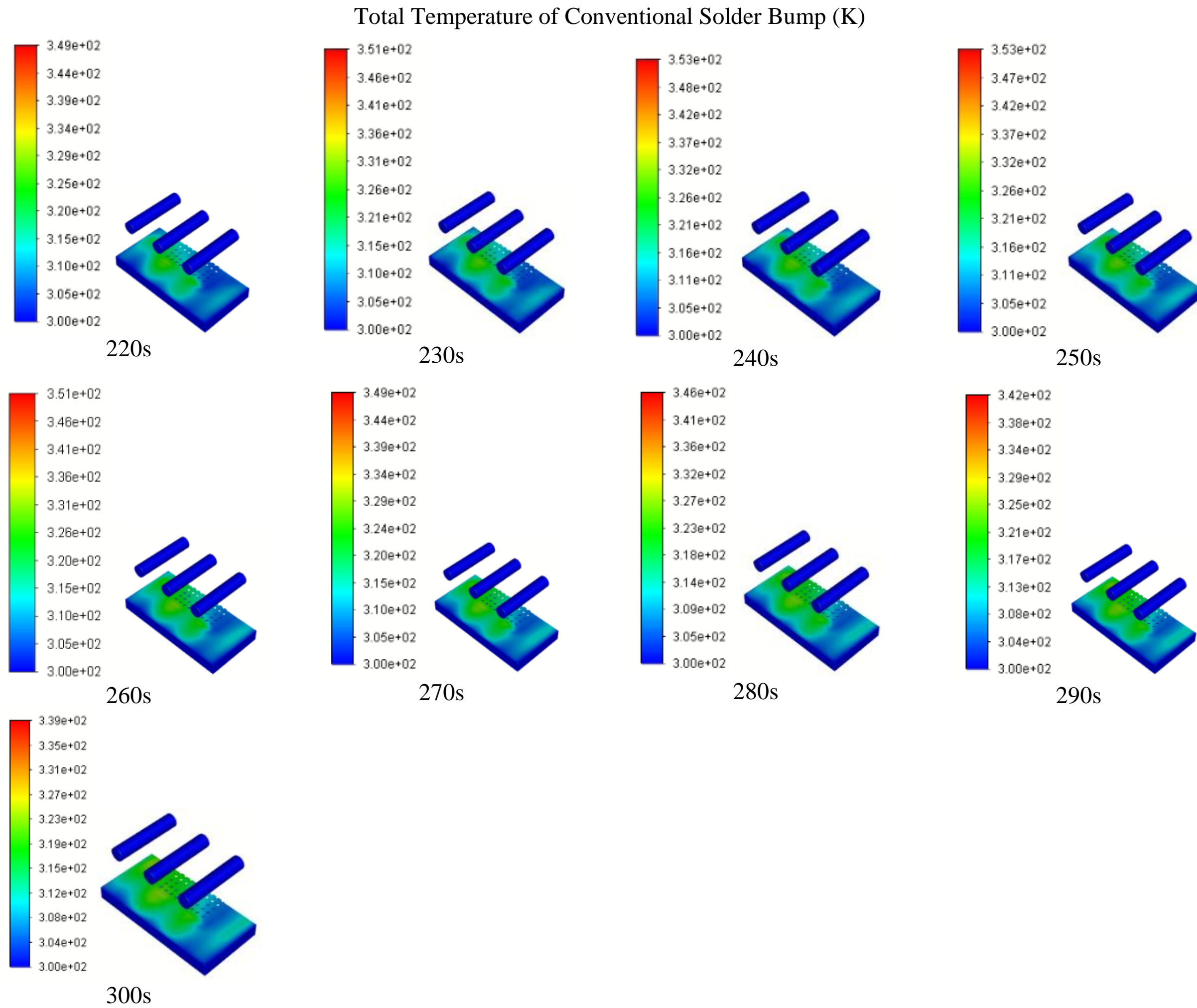


Figure 6: Temperature Distribution Contour Plot of Conventional Solder Bump (Isometric View)

Total Temperature of Copper Pillar Bump with Solder Cap (K)

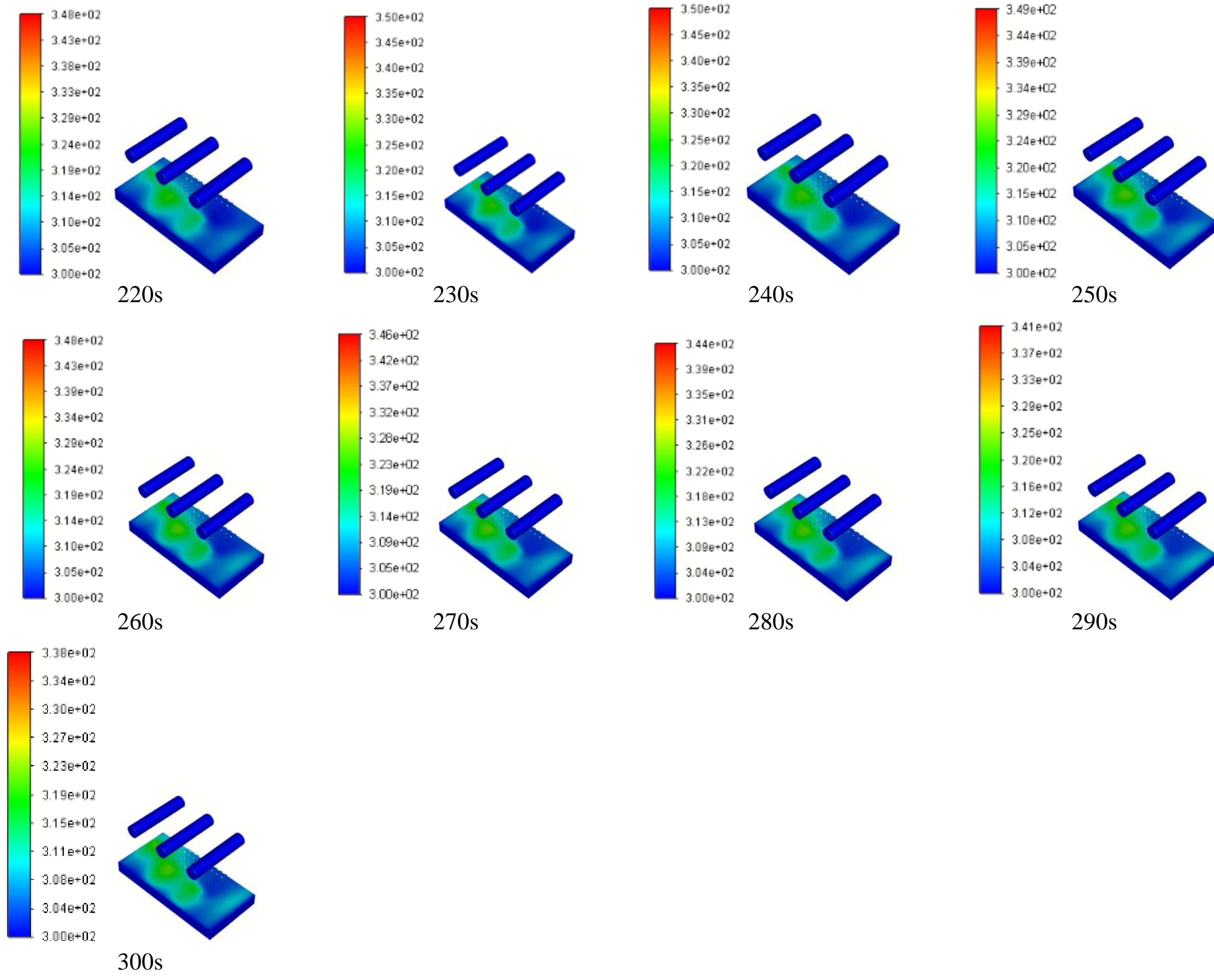


Figure 7: Temperature Distribution Contour Plot of Cu Pillar Bump with Solder Cap (Isometric View)

The highest temperatures of both convention solder bump and Cu pillar bump from reflow time 220s to 300s are tabulated the Table 6. From this table, it can be found that the peak temperature for conventional solder bump is 353K whereas for Cu pillar bump with solder cap is 350K. Throughout the simulation, it can also be seen that the temperature distributions of Cu pillar bump with solder cap are slightly lower than that of conventional solder bump.

Table 6: The Highest Temperature at Selected Periods

	Conventional Solder Bump									Copper Pillar with Solder Cap								
Time (s)	220	230	240	250	260	270	280	290	300	220	230	240	250	260	270	280	290	300
Highest Temperature (K)	349	351	353	353	351	349	346	342	339	348	350	350	349	348	346	344	341	338

Therefore, it can be concluded that both the interconnection bumps have been heated up in an even manner and this reduces the possibility of the interconnection joint failure. Besides that, when compared to conventional model, the Cu pillar model spent lesser time in the oven and thus saving cost and fuel as well as improve the quality of the solder joint.

Reflow Temperature Profile

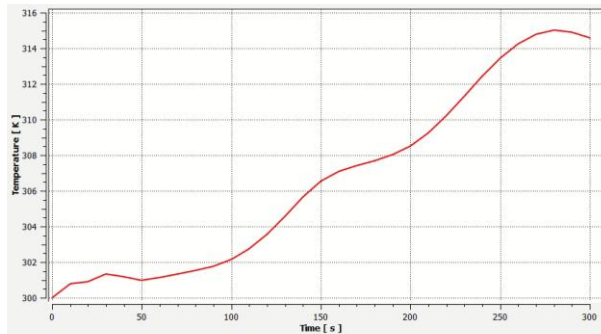
In the ANSYS Fluent Post-Processing, a central point at (x, y, z) = (0, 0, 0) is chosen to plot the temperature profile. This is because the symmetric point is located at the central point. Thus, the graphs of reflow temperature profile have been plotted as shown in Figure 8.

Based on the simulation result, the reflow time range for conventional solder bump is from 250s to 300s and more. The simulation running for 300s and the required time for conventional solder bump exceeds the 300s to complete a reflow soldering process. However, for Cu pillar bump with solder cap, the simulated reflow time range is from 215s to 300s, then continues with the cooling stage.

As a result, the simulation results allow the prediction of required time for the reflow soldering stage and also the peak reflow temperature of both conventional solder bump and Cu pillar bump with solder bump.

(a) Conventional Solder Bump

(b) Copper Pillar with Solder Cap



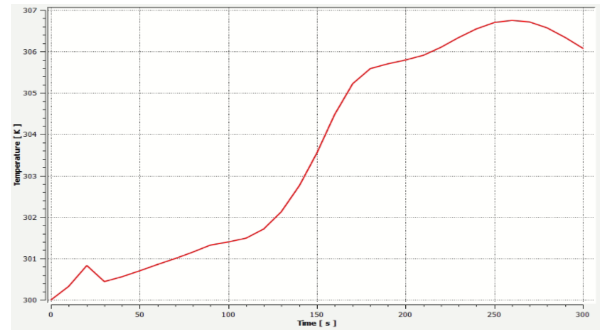


Figure 8: Reflow Temperature Profile (a) Conventional Solder Bump, (b) Copper Pillar with Solder Cap

CONCLUSION & RECOMMENDATION

As a result, the reflow temperature profiles of both conventional solder bump and copper pillar with solder cap are simulated through ANSYS Fluent. From the simulation, the time required for undergoing the reflow soldering stage and the peak reflow temperature are predicted. The results reveal that copper pillar bump with solder cap performs better than the conventional solder bump as it can save time and cost, as well as provide better interconnection joint quality.

In terms of improving simulation result, a mesh with high quality is critical to generate an accurate result. The grid independent test on the meshing elements of the simulation model is needed to check the consistency of temperature distribution and choose the most optimum case which is able to reduce the computational cost. Also, time step study is required to select the optimal time which can save the computational cost and provide realistic predictions.

In addition, the reliability of the interconnection joint can be tested and performed by different methods such as shear test, pull test and thermal shock test. Besides, the execution of the experiment is also important and required to validate the results generated from the virtual simulation. From the experiment, visual inspection with the help of electronic microscope can be used to examine the interconnection joints and their possible defects.

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